Properties and Synthesis of Passive, Lossless Soft-Switching PWM Converters.

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Abstract -- This paper derives general topological and electrical properties common to all lossless passive soft-switching converters with defined characteristics and proposes a synthesis procedure for the creation of new converters. The synthesis procedure uses the properties to determine all possible locations of the inductor and capacitor added to achieve soft switching. Then a set of circuit cells are used to easily add the additional circuitry to recover the energy stored in these elements. A family of soft-switching boost converters are given as an example of the synthesis procedure. Experimental waveforms are shown for a new soft-switching Cuk converter.

I. INTRODUCTION.

Higher switching frequencies allow reduction of the magnetic component sizes with pulse width modulated (PWM) switching converters. Unfortunately, increased switching frequencies cause higher switching losses and greater electro-magnetic interference (EMI). The switching loss mechanisms include: the current and voltage overlap loss during the switching interval and the capacitance loss during turn-on. The diode reverse recovery also causes an additional conduction loss and further contributes to the current and voltage overlap loss. Active or passive soft-switching methods have been used to reduce these switching losses. Recently, passive soft switching has received renewed inspection as a better alternative to active methods. Passive methods do not require an extra switch or additional control circuitry. They are less expensive, have higher reliability and have been reported to achieve higher performance/price ratios than active methods [1,2]. For PWM converters, passive soft switching reduces switching losses by lowering the active switch's di/dt and dv/dt to achieve zero-current turn on and zero-voltage turn off. Furthermore, by controlling the di/dt of the active switch, the reverse recovery current of the diodes are also controlled. The only loss mechanism not recovered with the passive technique is the energy in the internal capacitance of the switch. However, this loss is much smaller than the other switching losses and may be smaller than the loss incurred by using an auxiliary switch in an active method [1,2]. Historically, passive soft-switching techniques were used to reduce spikes in the switching circuits and were lossy by dissipating the recovered switching energy in resisters [3]. But more recently, many lossless and partially lossless techniques have been proposed [1,4-19].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor and capacitor. The inductor provides zero-current turn on of the active switch and limits the recovery current of the diodes while the capacitor provides zero-voltage turn off of the active switch. However, the topological rules that describe where these components must be place in the circuit have not been proposed in the literature. Typically the inductor and capacitor have been placed in series and parallel with the active switch respectively. But many other locations are possible and can lower the component count and reduce switch stress. Furthermore, additional circuitry accompanying the capacitor and inductor is used to recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. It is the objective of this paper to find general topological and electrical properties that describe these recovery circuits and the placements of the resonant inductor and capacitor to facilitate the creation of new circuits. Furthermore, circuit cells can be constructed that simplify the creation of new soft-switching circuits.

This paper derives general topological and electrical properties common to all lossless passive soft-switching converters with defined characteristics and proposes a procedure for the synthesis of new converters. The synthesis procedure uses the properties to determine all possible locations of the inductor and capacitor added to achieve soft switching. Then a set of circuit cells are used to easily add circuitry that recovers the energy stored in these elements. Section II describes the topological and electrical properties. Section III presents the synthesis procedure and gives examples. Section IV shows the experimental waveforms for a new Cuk converter created with the synthesis procedure. Section V concludes the paper.

II. TOPOLOGICAL AND ELECTRICAL PROPERTIES OF LOSSLESS PASSIVE SOFT-SWITCHING CONVERTERS

The development of any synthesis procedure must start with a thorough understanding and representation of the problem to be solved. Therefore, topological and electrical properties are derived that describe all PWM converters with passive lossless soft-switching characteristics.

A. Definitions of Lossless Passive Soft-Switching PWM Converters.

The definitions below first list the components that describe the hard switched PWM converter and then follow with additional components that are added to allow lossless passive soft switching. An essential element of isolated topologies, transformers, have been left out of the hard switched PWM components. Although not addressed in this paper they can be seen as an extension to the properties that follow.

Hard switched PWM converter:

1. A single DC voltage source, Vs.
2. A single linear time invariant (LTI) resistor R.
3. A set of LTI inductors $L = (L_i, i = 1,..., n_l)$
4. A set of LTI capacitors $C = (C_i, i = 1,..., n_C)$
5. A set of active switches $S = (S_i, i = 1,..., n_S)$, $n_s \geq 1$
6. A set of diodes $D = (D_i, i = 1, ..., n_d)$

Passive elements for lossless soft switching:

1. A set of zero-current inductors $Lr = (Lr_i, i = 1,..., n_{lr})$
   Lr provide zero-current turn on of active switches *S*.
2. A set of snubber inductors: $Ls = (Ls_i, i = 1,..., n_{ls})$
3. A set of zero-voltage capacitors $Cr = (Cr_i, i = 1,..., n_{Cr})$
   Cr provide zero-voltage turn off of the active switches *S*
4. A set of snubber capacitors $Cs = (Cs_i, i = 1,..., n_{CS})$
5. A set of snubber transformers $Ts = (Ts_i, i = 1,...,n_{ts})$
6. A set of snubber diodes $Ds = (Ds_i, i = 1,..., n_{ds})$

Voltage storage device (VSD)*: A VSD is a device or subcircuit that stores energy in the form of voltage. (e.g. capacitor, voltage supply, etc.)*

Passive turn-on and turn-off snubbers: *Sets of passive elements for soft switching that are added to the hard switched converter to limit the switch current and voltage during switch turn-on and turn-off intervals respectively.*

The definition of the hard switched PWM converter follows closely with the terms presented in [20,21] except for the treatment of active and passive switches. In the definitions above, the distinction is initially made between active and passive switches since it is assumed that the hard switched PWM topology and switch implementation has already been identified. Active switches *S* are implemented one of the three ways shown in Fig. 1 depending on possible directions of the switch *on current*, I_{on}, and the switch *off voltage*, V_{off}, following the convention in Fig. 1(a).

B. Lossless Passive Turn-On and Turn-Off Snubber Requirements.

A passive turn-on and turn-off snubber not only should slow the di/dt and dv/dt of an active switch respectively, but also losslessly recover the zero-current inductor (ZCL) and zero-voltage capacitor (ZVC) energy and maintain a manageable voltage stress across the switches and diodes. All these functions are executed during the switch transition interval (STI), a small resonant interval during the switch turn-on and turn-off transitions. The length of the switch transition interval is dependent on the switch speed, converter characteristics and size of the soft-switching components. The rest of the time, the converter is operating in the normal PWM converter mode. It is assumed that the snubbers do not change the PWM converter operation except at the small switch transition intervals at turn on and turn off.

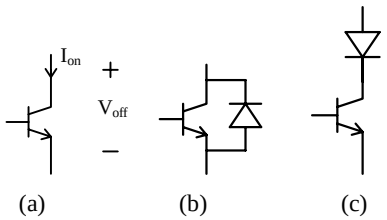


Fig. 1. Active switch implementation: (a) Transistor $I_{on}V_{off}>0$, (b) current bi-directional $V_{off}>0$, (c) voltage bi-directional $I_{on}>0$.

The main requirement of the turn-on snubber is to slow the switch current rise time. This is done by the insertion of a ZCL, Lr_i, into the circuit. However, this ZCL will store energy that must be recovered ultimately to the load, *R*, or the voltage source, V_s, to maintain lossless operation. This stored energy comes from two sources, the reverse recovery current of diodes D, and the PWM converter current from filter and/or energy transfer inductors *L*. In both cases, the snubber circuit must provide a conduction path when either a diode D_i or a switch S_i turns off. If no path is provided, either device can be destroyed by a voltage spike. Since an inductor stores its energy in the form of current which can increase converter conduction losses, it is desirable to transfer the ZCL energy to a VSD as soon as possible. Therefore, the energy recovery from the reverse recovery current of the diode should be performed as soon as the diode turns off (switch turns on). The recovery circuitry should also maintain a manageable voltage stress across the switches and diodes.

The main task of the turn-off snubber is to slow the switch voltage rise. This is done by the insertion of a ZVC, Cr_i, into the circuit. However, this capacitor will accumulate energy that must transfer to the load or the voltage source before the next turn-off interval. Because it is a passive circuit, this energy must be recovered when the switch S_i is turned on.

C. Zero-Current Turn On of Active Switches:

This subsection describes the number and placement of the ZCLs to allow zero-current turn on of all active switches.

Property 1. Zero-current inductor placements for single active switch PWM converters: *From a hard switched converter topology, a zero-current inductor Lr_i is placed in all loops comprised of S, and a nonempty subset of $(C \cup \{Vs\} \cup D)$ to achieve zero-current turn on of the active switch S.*

If *S* is in a loop satisfying the above condition then when *S* is turned on the switch current rises very rapidly while the switch voltage clamps to a nonzero value until the diodes complete their reverse recovery period. By inserting an inductor into this loop, the switch voltage can drop and the inductor sustains the voltage difference, which creates a controllable current slope. Additionally loops consisting only of *S* and *D* are assumed possible in PWM converters when implementing a current bi-directional switch. In this case both devices are represented as a single active switch *S*. As an example of property 1, Fig. 2 shows the boost converter with loop L_1 comprised of elements *S*, *D* and *C*. As shown, there are 7 possible placements of the ZCL to achieve zero-

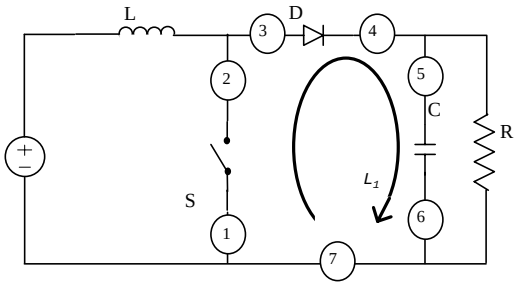


Fig. 2. ZCL locations for boost converter.

current turn on of switch *S*. Until now only locations 2 and 3 have been proposed for lossless passive soft-switching boost converters [1,4,5,6,7,8]. However, locations 1 and 4 are viable new placements of the resonant inductor. Although locations 5, 6, and 7 are new and will also provide zero-current turn on of *S*, they will adversely affect the load voltage and feedback control circuitry and so only locations 1-4 are proper. In any case one can see the ease of locating possible inductor locations by following property 1. The following property extends property 1 to include converters with more that one active switch.

Property 2. Zero-current Inductor placements for Multiple Active Switch PWM converters: *From a hard switched converter topology, a sufficient conditions for the zero-current turn on of S_i is a zero-current inductor, Lr_i, is placed in all loops comprised of S_i, a nonempty subset of $(C \cup \{Vs\} \cup D)$ and a subset (maybe empty) of S (excluding S_i).*

Applying property 2 to each switch of the full bridge or three phase voltage source inverter results in loops that have the input source, *Vs*, as a common element. This brings up the obvious result that only one resonant inductor can provide zero-current turn on for all switches. The following property summarizes this observation.

Property 3. Maximum number of zero-current inductors: *To provide zero-current turn on of X active switches, a maximum number of X zero-current inductors is needed.*

D. Energy Management For Zero-Current Inductors.

Energy collected in the ZCL from the reverse recovery current of a diode should be discharged when the diode turns off to minimize conduction losses. At the switch turn-off interval, the ZCL energy has several transition variations depending on the inductor's topological location. The most obvious case is when the ZCL is inserted in a branch containing a switch. In this case, when the switch turns off, the inductor energy must return to zero to minimize conduction losses. When the inductor is inserted in a diode branch that conducts complementary to the switch, the inductor energy must be charged at switch turn off. Finally, if the inductor is inserted in a non-switch or non-diode branch, the inductor energy will be discharged and then changed at switch turn off. In all these cases, an alternative conduction path must be provided to control (i.e. charge or discharge) the ZCL energy and eliminate large voltage spikes. There are many possible ways to control this energy transition, however all methods have similar topological and electrical properties.

Property 4. Management of inductor energy at either switch or diode turn off. *To control the energy in Lr regardless of whether a active switch or diode turns off, Lr_i must be in a loop comprised of a nonempty subset of Ds and a VSD. The voltage polarity of VSD and the conduction direction of Ds_i must be such that the inductor energy will transfer to and/or will charge from the VSD when a switch S_i turns off or a diode D_i recovers.*

Fig. 3 gives a conceptual example of the property 4 loop with a buck converter. Notice how the diode *Ds* is used to conduct the filter inductor current when *S* is turn off and the reverse recovery current, I_{rr}, when the diode recovers. Furthermore, the voltage polarity of V_{SD} is such that the inductor energy will be charged when *S* turns off and discharged when *D* recovers. The loop also ensures that the voltage stress across the switches and diodes are controlled.

As inferred from property 4, one mangagement loop is needed for each inductor. However, more than one energy management loop may be provided and may also contain a subset of $(S \cup D)$. In this case these loops are only effective for the turn off of diodes and switches not in the subset of $(S \cup D)$. The following special case of property 4 summarizes this observation.

Property 4 (special case) : *Loops comprised of Lr, the non-empty subset of Ds, a subset (maybe empty) of $(S \cup D)$ and a VSD can manage the inductor energy for the turn off of switches Si and diodes Di not in the subset of $(S \cup D)$.*

Property 4 (special case) gives additional guidelines for identifying and modifying inductor energy control loops for existing or new turn-on snubber circuits. Fig. 4 shows a new turn-on snubber that is operationally equivalent to [4,9] except it has different loops. When the diode *D* turns off, the recovery loop is *Lr-Ts-S-Ds1-Cs*, where *Ts* and *Cs* represent the VSD. When the switch turns off, the energy control loop is initially, *Ts-Lr-Cs-Ds2-Ds3* until *Cs* is drained to zero volts. Then the loop becomes, *Ts-Lr-D-Ds3* until diode *Ds3* turns off. Diodes *D*, *Ds2*, and *Ds3* can be in opposite directions to one another in the loops described above because a net inductor *L* current is always flowing toward the load.

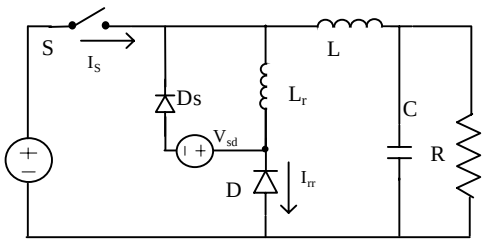


Fig. 3. Conceptual energy management example

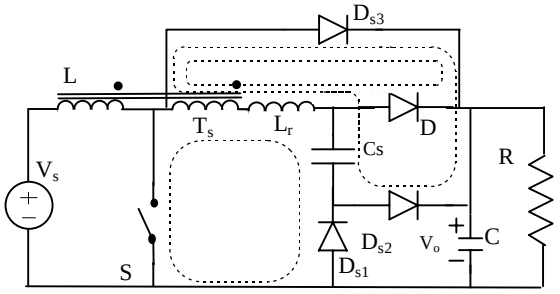


Fig. 4. A new circuit with multiple recovery loops.

This topological property also allows easy inspection of circuits claiming lossless operation. The circuits proposed in [6,7] are lossless only if the diode have no reverse recovery current. These circuits contain no loops satisfying property 4. Therefore, the ZCL energy from the reverse recovery current of the main diode will not be recovered and the voltage spike across this diode can be very large. For property 4, the VSD may be a relatively *stiff* voltage device where the voltage does not change much from cycle to cycle. Under these conditions, the next two subsections describe how this can be achieved.

1) Realization of VSD by a capacitor.

Because the inclusion of an additional power source is inconvenient for most applications, VSD can be realized by a relatively large capacitor from the set (*Cs* ∪ *C)*. This capacitor will accumulate energy from the ZCL each cycle. The energy accumulating in the capacitor also needs partial recovery each cycle to reach an equilibrium voltage. If VSD is from the set *C* only, then as shown in [8] this capacitor can be a filter capacitor for some PWM converter topologies (buck, Cuk, Zeta). For these select topologies the capacitor energy transfers directly to the load resistor. Otherwise the energy can be recovery by inserting a second inductor and diode so that an L-C-D circuit is in parallel with the an active switch or diode as shown in Fig. 5. With this arrangement, when the active switch (diode) is conducting the capacitor is transferring the energy to the inductor. When the active switch (diode) turns off the inductor will transfer this energy to the input source, load or energy transfer capacitors. The size of the additional inductor should be valued so that the additional conduction loss of the switch or diode is small. However as the inductor value is increased, the switch voltage stress becomes larger. In [8] an inductor is placed similar to

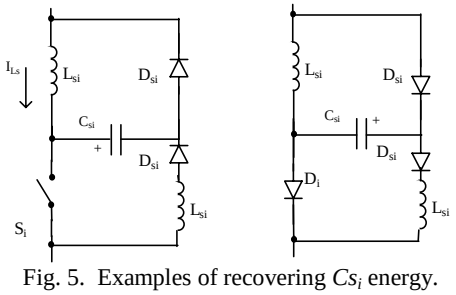


Fig. 5. Examples of recovering Cs_i energy.

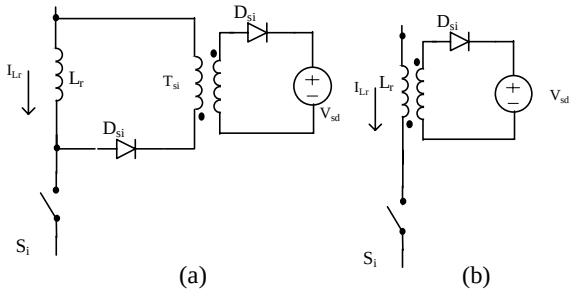


Fig. 6. Realization of VSD by transformer coupling: (a) forward transformer, (b) flyback transformer.

Fig. 5(b) without the additional diode. Without this diode, current can reverse direction in the inductor and increase the capacitor voltage rising the voltage stress of the switch and diode.

2) Realization of VSD by a transformer coupling.

A forward or flyback transformer coupling can be used to realize a VSD as shown in Fig. 6(a,b) for a switch. The advantage of transformer coupling is that the ZCL energy transfers each cycle directly to the bus voltage or other voltage storage element in the converter. The forward transformer method has been used for many proposed converters [10-17]. The flyback transformer was suggested in [3]. For either transformer coupling methods, the transformer leakage inductance can cause large voltage spikes when the switch or diode is turned off. Therefore, all proposed circuits also use some additional voltage clamping action (either lossy or lossless) to control this leakage inductance energy. References [4,6,9] and Fig. 4 show how the transformer can be coupled to the energy transfer inductor to realize a VSD.

E. Zero-Voltage Turn Off of Active Switches

Property 5. Zero-voltage capacitor Placement: *For zero-voltage turn off of the active switch S_i, S_i must be in a loop with a nonempty subset Cr, a subset of (C ∪ {Vs} ∪ Cs) and a nonempty subset of Ds. The diodes Ds in the loop must be in the direction to conduct the switch current when S_i turns off. The electrical requirement of this loop to ensure zero-voltage turn off is that when the switch S_i is opened and has zero parasitic capacitance, the voltage around the loop the moment after turn off must still be zero volts.*

The snubber components (*Cr*, *Cs*, and *Ds*) that make up the loop satisfying property 5 are defined as the *ZVC subcircuit*. The other elements in the loop are part of the original hard switching topology.

Property 6: Zero-voltage capacitor subcircuit placement (Using terms in graph theory [25]) *Every zero-voltage capacitor subcircuit represents a chord that creates a loop from the largest connected subgraph that contains switch Si and a subset of (C ∪ {Vs}). This subgraph is taken from the hard switched converter topology unless a zero-current inductor has been inserted into the topology. Then the*

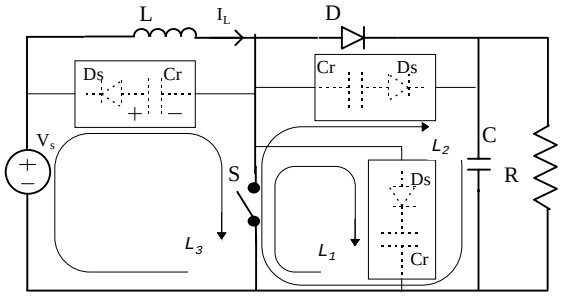


Fig. 7. Possible loops to achieve zero-voltage turn off of switch *S*.

subgraph is taken from the hard switched topology with the zero-current inductor Lr.

If property 6 is taken from the hard switched PWM converter topology, the resulting connected subgraph is a tree of the converter network as proved in [20]. If the subgraph is taken from the hard switched topology with the ZCL, since it is a subset of elements from the tree, it will also contain no loops (the *ZVC subcircuit* creates the loops). As an example of property 5 and 6, the boost converter in Fig. 7 shows the three different loops possible for the active switch *S* and the *ZVC subcircuits* shown in boxes. Take loop L_3 as an example and assume the switch has negligible parasitic capacitance. When the switch *S* turns off, the voltage across the capacitor *Cr* must equal the input voltage *Vs* so that the voltage around the loop equals zero volts. This ensures that the voltage across the switch increases from zero at the rate determine by the inductor current, I_L, and the value of capacitor *Cr*.

For passive soft-switching converters, the ZVC must be reset to a voltage satisfying the electrical requirement of property 5. The reset occurs when the active switch turns on. Furthermore, the energy in *Cr* must ultimately transfer to the input voltage source or the load of the converter to ensure lossless operation. An L-C resonance is the only method to losslessly transfer the energy in *Cr* toward a permanent storage device. However, there are several variations of L-C resonance and are shown in Fig. 8 with a boost converter. The reset circuits transfer the energy in *Cr* either to the input source or to another capacitor which completely or partially discharges to the load when the active switch turns off (the additional circuitry is not shown). The active switch is on when the reset period starts and assume that the inductor current is zero. The Fig. 8 caption describes how the energy transfer occurs for each reset circuit. For the reset circuit shown Fig. 8a, the ZVC voltage, Vcr, initially equals the output voltage Vo. The circuit resets Vcr to zero voltage by transferring all of the energy to the snubber inductor *Lr*. At this moment the energy in *Lr* transfers back to *Cr* until Vcr equals –Vcs. Then the energy is transferred to the parallel combination of *Cs* and *Cr*. Additional circuitry must transfer the energy in *Cs* to the load or the input. For the reset circuit shown in Fig 8b, the circuit operates very similarly except the inductor energy continuously transfers to *Cs* as Vcr discharges to zero. For the reset circuit shown in Fig. 8c, the energy in the capacitor transfers to the inductor, then back to the capacitor but with a different voltage polarity. Once the voltage across the capacitor equals -Vs, it is completely reset and the rest of the energy in the inductor transfers to the voltage supply Vs. Fig. 8c will not completely reset unless the initial capacitor voltage is greater than Vs. This limits the operating range of the circuit.

These reset circuits add additional current stress to the active switch. However since the resonant period can be designed to be small, the additional conduction losses are minimal. The following property describes the upper limit of ZVCs needed to satisfy property 5.

Property 7. Maximum number of zero-voltage capacitors: *To provide zero-voltage turn off of X active switches, a maximum number of X zero-voltage capacitors Cr is needed.*

F. Minimal Active Switch Voltage Stress

Property 8. Minimum Active Switch Voltage Stress: *To maintain a minimum voltage stress across an active switch when the zero-current inductor Lr is inserted adjacent to a diode D_i, at least one auxiliary diode Ds must provide the same path from the active switch to the subset ($C \cup Vs$) as the hard switched topology diode D_i did. Additional circuitry must ensure that the additional diodes Ds stops conducting before the active switch is turned on, so that zero-current turn on is realized.*

The ZCL inserted into the circuit using property 1 no longer allows the turn-off transition of the active switch to be clamped to a voltage supply through the diodes *D*. Therefore, to maintain the minimal voltage stress across the active switch, a separate snubber diode current conduction path must reproduce the original conduction path that the diode *D*

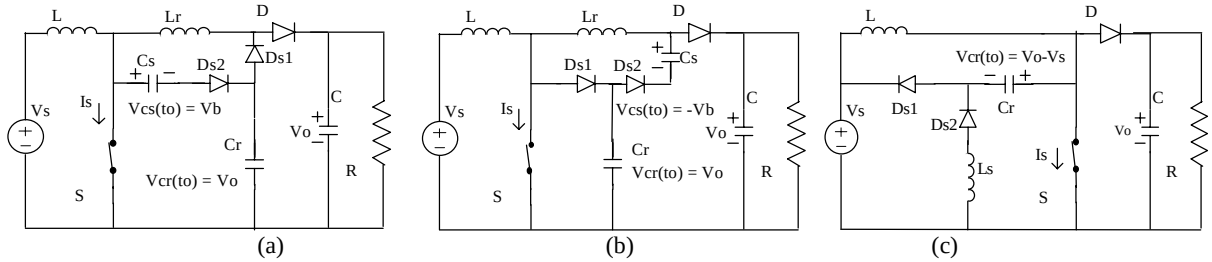


Fig. 8.Possible Reset Circuits (a) energy flow *Cr⇒Lr⇒Cr while (Vcr>-Vcs) then Lr⇒Cr & Cs*, (b) energy flow *Cr⇒Lr & Cs⇒Cs*; (c) energy flow *Cr⇒Ls⇒Cr* while (Vcs > -Vs) then *Ls⇒V_s* (Vcs= -Vs)

allowed before inserting the inductor *Lr*. Additionally, the property points out that some placements of the ZCL that do not allow the application of property 8.

III. SYNTHESIS OF PASSIVE LOSSLESS SOFT-SWITCHING CONVERTERS

The topological and electrical properties from Section II simplify the synthesis of lossless passive soft-switching PWM converters. The synthesis process is described for a group of single active switch DC-DC converters and may be extended to converters with more than one active switch. From property 3 and property 7 and the fact that there is only one active switch, only one ZCL and ZVC provide zero-current turn on and zero-voltage turn off of the active switch respectively. The locations of the turn-on inductor *Lr* and the turn-off capacitor *Cr* are described as the *basic* soft-switching topologies for a given hard switched converter. These *basic* topologies describe all passive soft-switching circuits originating from a given hard switched converter. Additional lossless passive components then need to be included to ensure the energy from the ZCL and ZVC is recovered. The number of additional components and their interconnections are virtually limitless. However, this paper proposes several circuit cells that can take each *basic* topology and realize a lossless soft-switching converter. The steps in the synthesis procedure are as follows:

Step 1*: Take the element intersection of all loops satisfying property 1. From this set eliminate filter capacitors and the input power source Vs to obtain L_{loc} elements where the inductor can be inserted in series. The number of possible zero-current inductor locations is then $2L_{loc}$, by inserting the inductor on either side so it makes a cutset with the element.*

Step 2*: For each inductor location of step 1, identify the locations of the zero-voltage capacitor subcircuit using the topological part of property 5. Using the subgraph defined in property 6, the number of locations can be found by defining the number of elements in the subgraph on either side of switch S_i as E_1, and E_2, respectively. The number of capacitor subcircuit locations is a follows:*

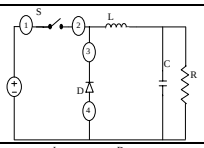
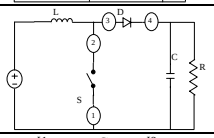
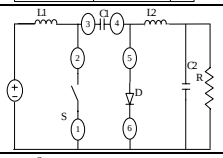
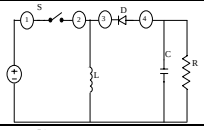
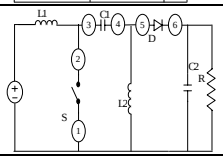
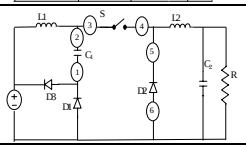
$$C_{loc} = (1 + E_1)(1 + E_2) \qquad (1)$$

These inductor and capacitor subcircuit locations make up the <u>basic</u> soft-switching topologies.

Step 3*: For each <u>basic</u> topology match one or more of the given circuit cells to the ZCL and ZVC subcircuit locations to ensure the rest of the topological and electrical properties are satisfied.*

Table 1 describes the *basic* topologies for a group of single switch DC-DC converters using steps 1 and 2 of the synthesis procedure. For each hard switching converter, the reasonable ZCL locations are shown. The ZCLs are not inserted into the loop between the filter capacitor and load resistor, or along the ground plane as discussed in Fig. 2. Then for each ZCL location, the number of possible *ZVC subcircuit*s is listed. For example, ZCL location one of the boost converter, labeled L1, has only one *ZVC subcircuit* placement. Therefore, the table entry for this location is L1-1. The total number of *basic* topologies is also listed for each converter.

Table 1
BASIC SOFT-SWITCHING TOPOLOGIES FOR A GROUP OF DC-DC CONVERTERS

	***Lr* locations**	***Cr* Locations**	**Total**
Buck		L1-1, L2-3, L3-3,L4-3	10
Boost		L1-1, L2-3, L3-3, L4-3	10
Cuk		L1-2, L2-3, L3-3, L4-6, L5-6, L6-6	26
Buck-Boost		L1-1, L2-3, L3-3, L4-3	10
Sepic		L1-2, L2-3, L3-3, L4-6, L5-6, L6-6	26
Buck Quad-ratic		L1-2, L2-1, L3-1, L4-2, L5-2, L6-2	10

Once a *basic* topology is identified, one or more circuit cells is used to provide the additional circuitry to satisfy all the properties. Figs 9 shows two circuit cells that satisfy the pertinent turn-on and turn-off properties and also provides minimum voltage stress across the active switches (property 8). Among them, cell I has not been proposed in the literature. Cell II can be used to create a soft-switching boost converter shown in [5]. In the circuit cells, *Lr* and *Cr* are the ZCL and ZVC to satisfy properties 1 and 5. *Ds1* and *Cr* make up the *ZVC subcircuit*. *Lr* also transfers the energy in *Cr* to *Cs*. *Cs* recovers the energy in *Lr* (property 4) and *Cr* (property 5). Diodes *Ds1*, *Ds2*, *Ds3* transfer the energy in *Cs* to the load or energy transfer capacitor each switching period and also satisfy property 8. Fig. 10 shows four circuit cells (i.e. cells III, IV, V, VI) that satisfy the pertinent turn-on and turn-off snubber properties but do not maintain the minimum voltage stress across the switch (property 8 not satisfied). For these cells *Cs* is a relatively large capacitor and stores the

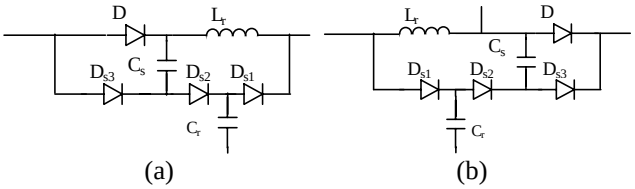


Fig. 9. Circuit cells satisfying property 8. (a)Cell I; (b)Cell II

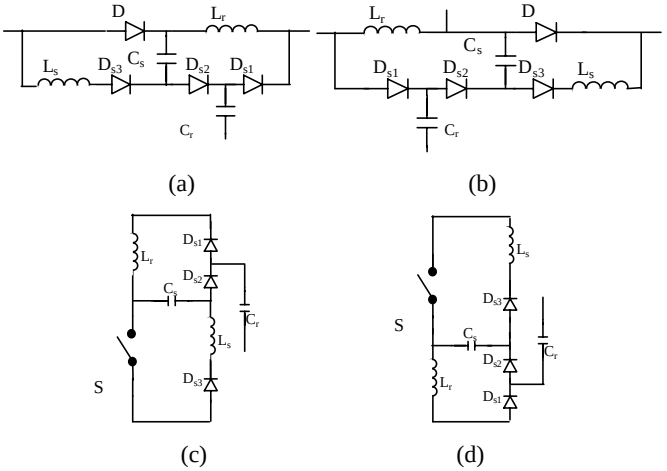


Fig. 10. Circuit cells using a capacitor to reset inductor Lr. (a) Cell III; (b)Cell IV; (c)Cell V; (d)Cell VI.

inductor *Lr* and capacitor *Cr* energy from cycle to cycle. Elements *Cr*, *Cs*, and *Ds2* comprise the *ZVC subcircuit*. *Ls* is relatively large and transfers the energy in *Cs* to a subset of ($C \cup Vs$). Cells III and IV can be used to create converters similar to ones presented in [8], however cells V and VI are new. All cells in Figs. 9 and 10 become just turn-on snubbers by removing the capacitor *Cr* and a diode *Ds1*. Cells V and VI become just turn-off snubbers by not placing inductor *Lr* into a loop satisfying property 1. Most *basic* topologies require only one circuit to provide complete soft switching. However, a few *basic* topologies must use two circuit cells, one for a turn-on snubber and one for a turn-off snubber. Cell V needs a slight modification to work as a turn-off snubber when realizing two *basic* topologies of the Cuk and Sepic converters and one *basic* topology of the buck quadratic converter. For these topologies the energy transfer capacitor, *C*, is inserted into the branch containing *Cs* so it make a cutset with *Cs*.

Fig 11 shows the synthesis procedure results for the boost converter. It shows a set of soft-switching circuits, one for each *basic* topology. Each circuit provides both zero-current turn on and zero-voltage turn off of the active switch. Seven of the 10 circuits provide the active switch with the same voltage stress as the hard switched converter (property 8). Fig. 11a shows the circuit created using inductor location L1 and the circuit cell VI. Fig. 11b shows three circuits created using inductor location L2 and the circuit cell II. Each different capacitor *Cr* connection creates a different *ZVC subcircuit* location. Fig. 11c shows three circuits created using inductor location L3 and also uses circuit cell II. Here

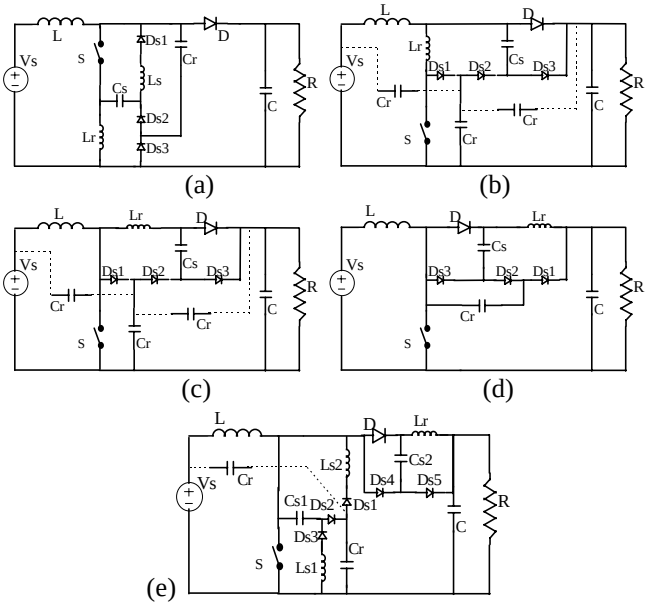


Fig. 11. Synthesis results for the boost converter. (a) location L1-1 (b) locations L2-3 (c) locations L3-3 (d) location L4-1 (e) locations L4-2.

the circuit cell is inserted into the converter slightly differently to adjust for the different inductor location. Fig. 11d shows one circuit created using inductor location L4 and cell I. No other placements of the capacitor subcircuit are possible with this circuit cell. Therefore, Fig. 11e shows the additional two *ZVC subcircuit* locations for inductor location L4. These locations require two circuit cells. The turn-on snubber uses a modified version of Cell I (no Cr and Ds1) and the turn-off snubber uses Cell V.

IV. A NEW SOFT-SWITCHING CUK CONVERTER.

Experiments with a new soft-switching Cuk Converter shown in Fig. 12 verified theoretical operations. The experimental circuit operated with the following parameters: Fs= 100kHz, V_s = 50v, V_o = 100v, P_{out} = 100W, *Lr* = 4uH, *Cr* = 5nF. Fig. 13 shows the experimental waveforms. Fig. 13a shows the switch voltage and the I_{Lr} current. Notice that the voltage stress across the switch is still 150 volts, the same as the hard switched converter. When the switch turns on the inductor *Lr* resets the *Cr* capacitor voltage to provide zero-voltage turn off. Fig. 13(b) shows how *Lr* slows the switch

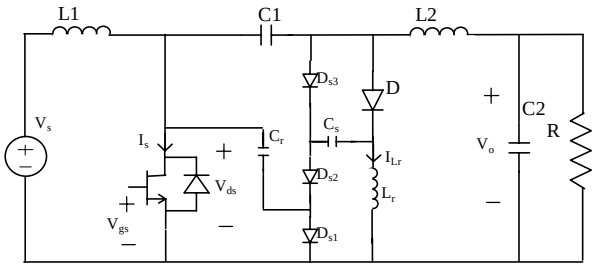


Fig. 12. A new lossless passive soft-switching Cuk converter.

current at turn on. The small current hump at the start is attributed to parasitic diode *Ds1* capacitance that must be charged. Fig 13(c) shows how *Cr* slows the switch voltage rise at turn off.

V. CONCLUSION.

This paper studies properties common to all lossless passive soft-switching converters that achieve the requirements cited in section IIb. Furthermore, property 8 describes soft-switching converters that do not increase the voltage stress compared to the hard switched converter. These properties ease the development of a synthesis procedure for the creation of new converters. For a number of ZCL and *ZVC subcircuits* a complete set of *basic* soft-switching topologies are defined for a given hard switched converter. This set of *basic* topologies describes all passive soft-switching converters for a given hard switched converter. Additional circuitry then needs to ensure the energy stored in these passive elements is recovered. The possible number of circuits to achieve this result is almost limitless, however, they also have many common properties. A set of circuit cells are then described that can be used to synthesis a family of soft-switching converters. As an example, 10 soft-switching boost converters are given and one soft-switching Cuk converter was shown with experimental results.

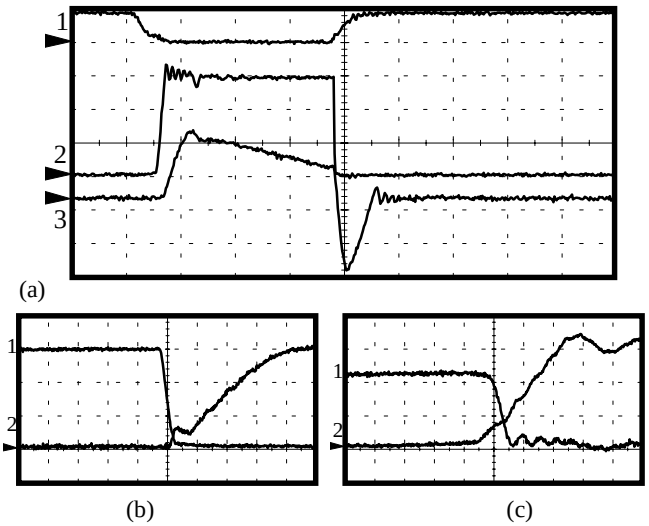


Fig. 13. Experimental waveforms for Cuk Converter. (a) Switching cycle. 1: V_{gs} 20v/div; 2: V_{ds} 50v/div; 3: I_{Lr} 2amp/div; horizontal scale: 1us/div. (b) Switch turn on. 1: Vds 50v/div; 2: Is 2amp/div; horizontal scale: 50ns/div (c) Switch turn off. 1: Is 2amp/div; 2: Vds 50v/div; horizontal scale: 50ns/div

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